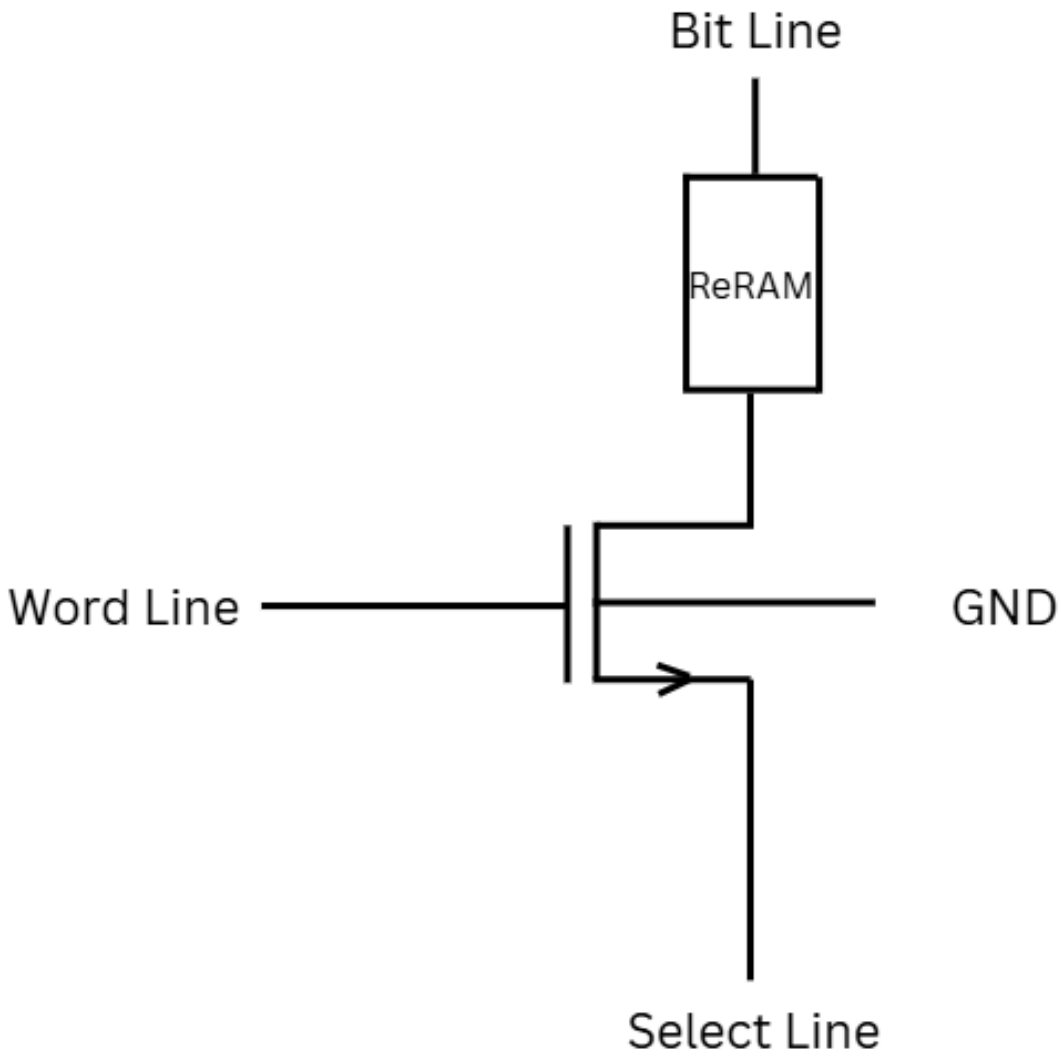
High Level Design Process and Discussions

Designing for Characterizations



1.0 Investigation: Device Physics & Process Variation

Goal: To quantify how ReRAM resistance and switching behavior change with physical size and location on the die.

Primary Method (Off-Chip Control): All 48 terminals (16 cells x 3 terminals: WL, BL, SL) would be pinned out to pads (This may need to be cut down). This complete electrical access allows external test equipment to perform precise I-V sweeps and gather statistical data on resistance distributions, enabling direct comparison between the different size and location groups

Test Structure (Process & Size Variation Array): A 16-cell array of individual 1T1R structures, organized into four groups of four cells.

- Group 1: 4 cells with a **minimum-sized** ReRAM layout.
- Group 2: 4 cells with a **medium-sized** (2x area) ReRAM layout.
- Group 3: 4 cells with a **large-sized** (4x area) ReRAM layout.
- Group 4: 4 cells with a **minimum-sized** ReRAM layout, placed physically distant from Group 1.
- **Stretch Goal (On-Chip Control):** A dedicated 1T1R cell will be connected to an on-chip, digitally tunable LDO or a 2 or 4-bit DAC to demonstrate on-chip voltage generation for FORM/SET/RESET operations

2.0 Investigation: Programming Dynamics & Endurance

Goal: To characterize the impact of programming pulse parameters (voltage, duration) on the cell state, and to measure the cell's operational lifetime (endurance).

Primary Method (Pulse Dynamics): An external precision pulse generator will be connected to the pads of the array's cells to sweep a wide range of pulse widths and voltages. The resulting cell state will be read externally to create detailed device "tuning curves" as described in the documentation.

Primary Method (Endurance): External equipment will be used to apply millions of repeated SET/RESET cycles to a subset of the array's cells. The cell state will be monitored for failures (e.g., stuck-at-LRS or stuck-at-HRS) to determine the average number of cycles before breakdown.

Test Structure: The "Process & Size Variation Array" (from Sec 1.0) will be used for primary testing.

Justification: The official Sky130 ReRAM documentation highlights that programming is a complex process. The technology specifications describe using different voltages as "tuning knobs," and the background documentation explicitly lists "limited endurance" as a key design challenge.

Stretch Goal (On-Chip Automation): Design a dedicated "Endurance Test Module" consisting of a small array (e.g., 4x4) and an on-chip controller to autonomously cycle the cells and log failures, enabling high-speed, long-term endurance testing that is impractical with external equipment.

3.0 Investigation: Array Scalability & Signal Integrity

Goal: To measure the IR drop (voltage droop) across bit/source lines of varying lengths to understand the scaling limits of ReRAM arrays.

Primary Method (Off-Chip Measurement): The extensive pin-out allows for precise external control. One can select a specific cell by activating its word line, then force a current through one end of the bit line and sense the resulting voltage at the other. This provides a direct and accurate measurement of the voltage droop under a specific load condition.

Test Structure (Column Droop Test Structures): Two dedicated columns of 1T1R cells: one short (e.g., 8 cells) and one long (e.g., 32 cells). For each column, the shared bit line will have pads at both ends, and every word line for each cell will be pinned out to a dedicated pad.

Stretch Goal (On-Chip Compensation): Integrate a Line Driver with selectable output strength at the head of the long column structure. This will allow for testing of on-chip IR drop compensation schemes by digitally adjusting the drive strength to counteract the measured droop.

4.0 Investigation: System Integration & Functionality

Goal: To characterize the building blocks of a full system and demonstrate a functional compute-in-memory subsystem.

Primary Method (Component-Level): Characterize the Standalone Analog Blocks and the Bare Crossbar Array independently to establish baseline performance for the analog components and the passive array before they are integrated.

Test Structures:

- **Standalone Analog Blocks:** A TIA, a 1-bit ADC (comparator), and a 1-bit DAC. A stretch goal is also to include 2-bit or 4-bit ADC/DAC versions. All critical I/O will be pinned out for isolated characterization.
- **Bare Crossbar Array:** A 2x2 and/or 4x4 crossbar array of 1T1R cells. This structure will not include on-chip peripherals; instead, all word lines, bit lines, and source lines will be directly connected to pads, allowing for external control and debugging of the array structure itself.

Stretch Goal (System-Level): Design and fabricate a fully integrated 2x2 or 4x4 crossbar that combines the 1T1R cell layout with the TIA, DAC, and ADC to perform a verifiable read or Multiply-Accumulate (MAC) operation.

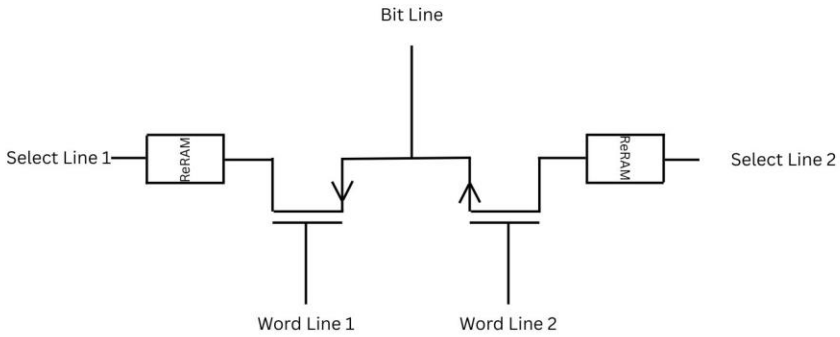
5.0 Investigation: ReRAM 1T1R NMOS/PMOS Setup

Goal: To characterize different setups of the 1T1R using NMOS and PMOS transistors

Primary Method(Off-Chip meassurement): Observe is there is any benefit regarding latency, die area and/or stability. Compare the results of applying the same inputs into a standard NMOS 1T1R setup, and the results of applying the same input to the setup with NMOS & PMOS. Is there a difference in the outputs? What was the latency difference?

Test Structures: Wire the drains of a NMOS & PMOS transistors in series and connect it to the Bit Line (the input). The Resistor of each cell is connected to the source of each respective transistor. The Word Line is still connected to the gate of the transistors.

Stretch Goal (System-Level): Try to produce different possible NMOS & PMOS setups to test with the ReRAM



6.0 Optional Modules for Exploratory Research

Exploratory Area: Thermal Effects

- **Goal:** To characterize the impact of temperature on ReRAM data retention and switching behavior.
- **Justification:** The referenced SPICE compact model is based on Joule heating and temperature-dependent physics, and the Sky130 ReRAM background documentation warns of "retention challenges at very high temperatures."
- **Potential Module:** A "Thermal Test Structure" consisting of 1T1R cells placed adjacent to an on-chip resistive heater and a temperature sensor.

Exploratory Area: Multi-Device Cell Interactions

- **Goal:** To investigate the "write/read disturb" phenomena in denser 1T(n)R cell configurations.
- **Justification:** The Sky130 ReRAM technology specifications dedicate a section to this issue, noting that programming one cell can disturb its neighbors and suggesting "compensating SET operations" as a solution.

Prioritizing Requirements

- Primary (Non-Negotiable) Goals
- Secondary Goals
- Tertiary (Stretch) Goals

- Goal: Fabricate all test structures and perform full **off-chip characterization** to validate device physics, scaling limits, and component baselines.
- Goal: Design **on-chip automated** circuits to execute key characterization tasks (e.g., programming, endurance) internally.
- Goal: **Integrate** validated blocks into a functional subsystem (Compute Crossbar) and explore advanced, high-risk experimental modules.

Primary Requirements: Off-Chip Characterization

Modules:

- Core Device Array (Single ReRAM Cells Min, Med and Large 1T1R's, 1S1R's)
- Array Structures (Droop Columns, Bare Crossbar)
- Standalone Mixed-Signal Blocks (TIA, ADC, DAC, Analog MUX's)

Key Tests & Goals:

- Programming Dynamics: Find FORM/SET/RESET "tuning curves"
- Endurance: Cycle-to-failure testing
- Statistical Analysis: R_{LRS} / R_{HRS} distributions
- IR Drop Measurement: Quantify voltage droop under load
- Analog Baselines: Characterize TIA gain/BW, ADC offset, etc.

Secondary Requirements: On-Chip Automated Testing

Modules:

- On-Chip Programming Logic (1T1R cell + on-chip tunable LDO/DAC)
- Automated Test Modules (Endurance Controller + Array)
- On-Chip IR Droop Compensation (Selectable Line Driver)

Tests:

- On-Chip Programming: Validate internal generation of FORM/SET/RESET pulses
- Automated Endurance: Enable autonomous, high-speed cycle-to-failure testing
- Active IR Compensation: Quantify on-chip droop correction under load

Tertiary Requirements: Full System & Exploratory

Modules

- Integrated Subsystem (Full 2x2/4x4 Compute-Crossbar)
- Exploratory Structures (Thermal, Device Interaction, Parallel Drive Lines)

Key Tests & Goals

- System-Level Operation: Perform verifiable Multiply- Accumulate (MAC) operation
- Thermal Analysis: Characterize temperature's impact on retention/switching
- Disturb Effect Analysis: Quantify read/write disturb phenomena

Key Constraints & Design Hurdles

What are some limitations of the chip that will impact our test structures?

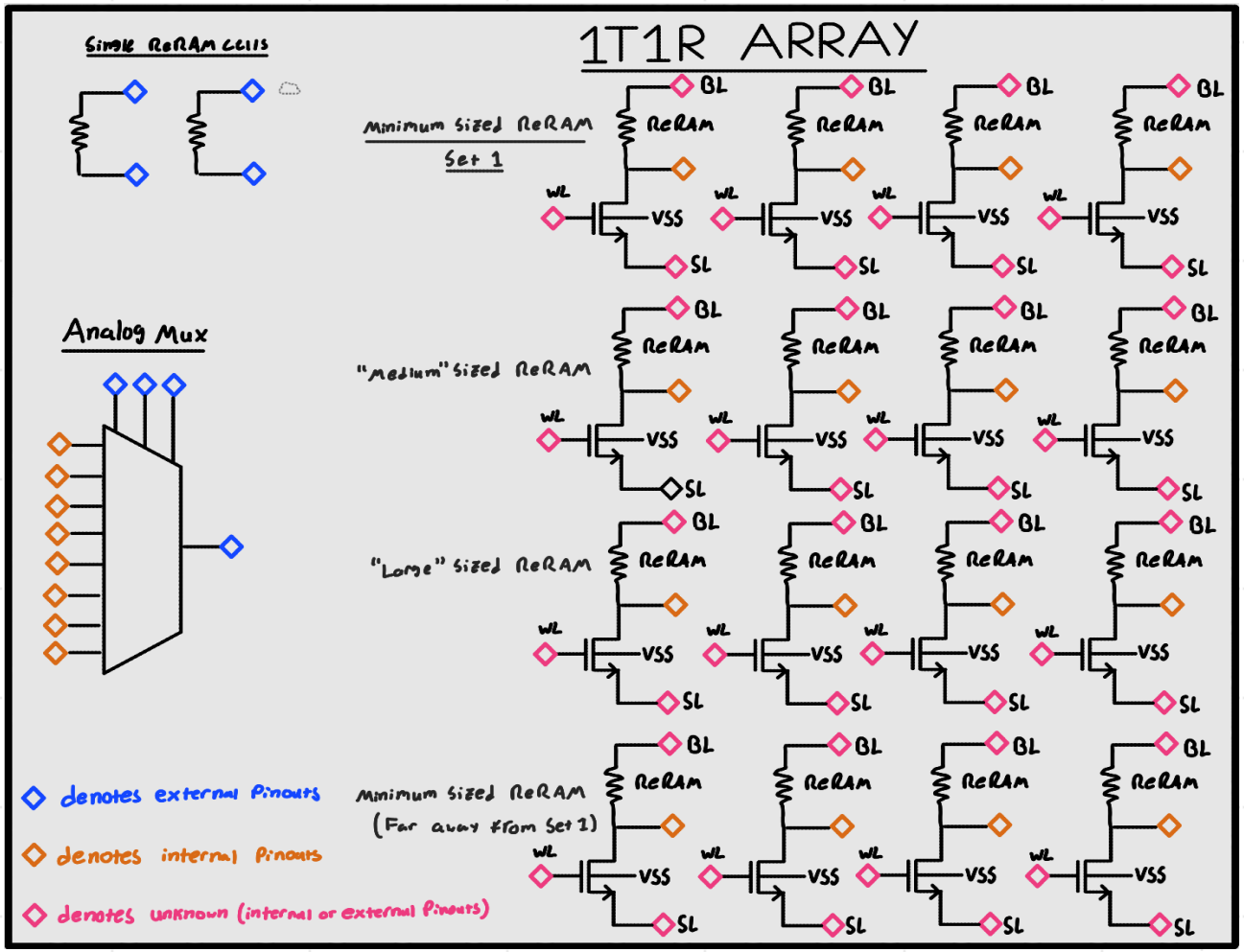
- Pad/Pin Limitation
  - What is the exact number of available I/O pads?
    - Constraint will dictate the maximum number of signals we can test concurrently.
- Analog Muxing Requirement
  - Given the 48+ terminals for the main array, extensive analog multiplexing is a non-negotiable.
  - Must design and validate a simple, reliable analog mux.
- Pad Frame & I/O Restrictions
  - Are there specific pads for analog vs. digital signals?
  - Must investigate ESD protection limitations and potential noise coupling between adjacent pads.
- Internal vs. External Control
  - Pin limitations will force us to decide what *must* be external (e.g., precision analog nodes) vs. what *can* be internal (e.g., mux select lines driven by a shift register).

Primary Requirement Designs

Proposed modules for basic externally driven tests and characterization

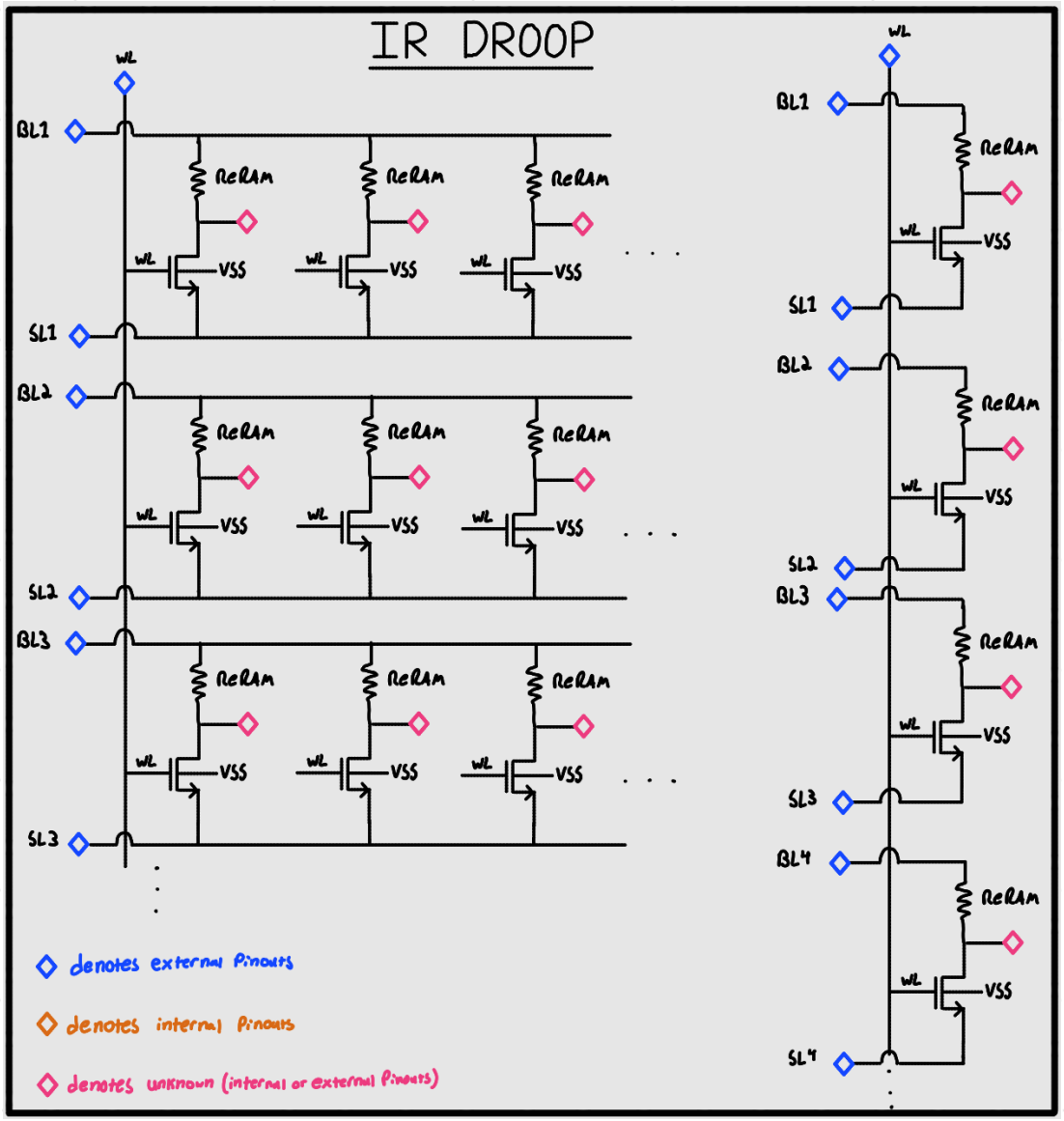
Core ReRAM Characteristic Modules

Some of the most basic designs to understand the behavior of individual ReRAM Cells – Standalone Cells, 1T1R Array, Varied Sizes



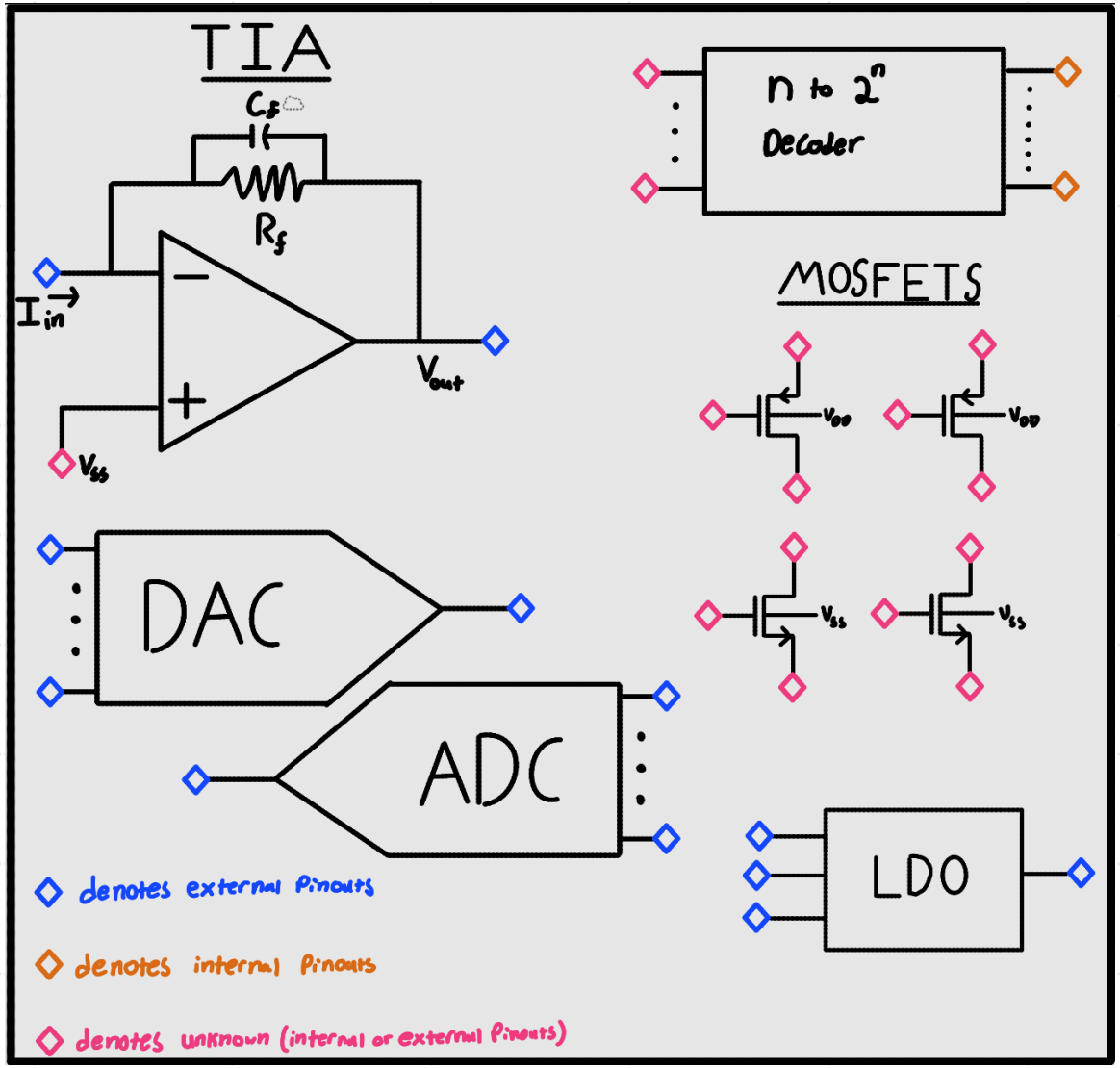
IR Droop and Bare Crossbar Characterization

Determine the loss through columns or rows of 1T1R cells of varying lengths to investigate scalability concerns



Standalone Mixed-Signal Blocks

Learn how standard building blocks behave in silicon relating to noise, offset, and module specific parameters



Secondary Requirement Designs

Proposed modules for internally driven tests and characterization